AMENDMENTS TO THE SPECIFICATION

Please delete paragraph [0003] and replace with the following:

[0003] WO 99/43131 discloses in detail algorithms to be used by the control unit to determine which respective output port to connect to each input port in each switching cycle. Each cell of data is associated with a priority level, and each ingress router operates a VOQ for each output port and priority level. Each VOQ is for storing cells of the corresponding priority level and destined for the corresponding output port. When a new cell arrives at an ingress router, it is placed in the appropriate queue, and a request for a connection between the corresponding input and output ports is passed to the control unit. To process these incompatible requests, the control unit performs an arbitration process which includes a first pipeline stage to satisfy at least some of the requested interconnections. A priority mixer of the control unit receives those requests for interconnections which were not satisfied by the first pipeline stage together with requests of a different priority level. The priority mixer operates to select which of those requests should be further considered and applied to a second pipeline stage. This is second pipeline stage is operable to satisfy such of those requests as are possible. Further pipeline stages are provided, to which are applied those requests not satisfied by any preceding pipeline stages.

Please delete paragraph [0016] and replace with the following:

[0016] A processor may further be further provided at each egress router, for re-converting the format of cells which have passed through the switch into a standard TDM traffic format. In many systems, each ingress router is associated with a respective egress router, and in this case the two processors may be provided within a single processor unit.

Please delete paragraph [0026] and replace with the following:

[0026] Each of the ingress routers IR.sub.0 to IR.sub.n receives data from two input buses, labelled A and B. Input bus A, which may be a conventional <u>common switch interface (CSIX)</u> or Intel <u>Internet exchange bus (IXBus)</u>, transmits data cells to the corresponding ingress router at times which are not predefined. The ingress router is provided with VOQs for each of the egress routers ER.sub.0 to ER.sub.n and priority levels (i.e. the number of VOQs is equal to n+1 times the number of priority levels). It is further provided with at least one multicast VOQ, for storing data cells which arrive at times which are not predefined and are intended for broadcast to multiple egress routers. A cell of data including a header is commonly referred to as a "tensor", and is composed of a number (e.g. 6 or 8) of "vectors", where a vector consists of one byte per plane of the switching matrix and is transferred though it in one system clock cycle.